

IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A quantizer (4) for a sigma delta modulator (10) with at least one input stage (2), the quantizer (4) quantizing an input signal (24), which is present at its input stage, in accordance with at least one threshold signal (25) and outputting it as result value (22) at a digital result output (23), characterized in that the quantizer (4) contains at least one quantizing cell (40) corresponding to the number of its resolution levels, each quantizing cell (40) having an input voltage/current converter (41; ~~41a and 41b~~), which converts the input signal (24) to be quantized into a corresponding input current (42), to the at least one quantizing cell (40), a static threshold current source (~~49a and 49b~~) is allocated which supplies a static component to the threshold signal (25) in the form of a static threshold current (~~I_{ref}~~), that a dynamic feedback current source (44; ~~44a and 44b~~) is provided which generates a feedback current (~~45; 45a, 45b; I_{dae}~~) derived from the digital result value (22), which feedback current is added to the static threshold current (~~I_{ref}~~) in a current node (~~46; 46a and 46b~~), that the threshold current composed of static threshold current and feedback current is added to the input current in the current node (~~46; 46a and 46b~~), that a comparison unit (47) is provided which decides whether the accurate current present at the current node (~~46; 46a and 46b~~) is not equal to zero and supplies a digital result accordingly.
2. (Currently Amended) The quantizer as claimed in claim 1, wherein, for obtaining the analog feedback current (45) derived from the digital result value (22), a digital/analog converter (3) is provided which supplies a voltage signal (~~I_{N-DAC}~~) corresponding to the result value for deriving the feedback current.
3. (Currently Amended) The quantizer as claimed in claim 2, wherein the digital/analog converter (3) is constructed in such a manner that it supplies the feedback current (45) directly as analog output signal.
4. (Currently Amended) The quantizer as claimed in ~~one of the preceding claims~~ claim 1, wherein the input voltage of the current converter (41; ~~41a and 41b~~) is a transistor (~~411a and 411b~~) driven at a base input by means of the input signal.

5. (Currently Amended) The quantizer as claimed in ~~one of the preceding claims~~ claim 1, wherein each quantizing cell (40) is allocated a threshold signal which differs from the threshold signals of other quantizing cells.
6. (Currently Amended) The quantizer as claimed in ~~one of the preceding claims~~ claim 1, wherein the threshold signals exhibit fixed differences with respect to one another.
7. (Currently Amended) The quantizer as claimed in ~~one of the preceding claims~~ claim 1, wherein an amplifying stage (48) is provided which amplifies the current at the current node (~~46; 46a, 46b~~) before it is weighted by the comparison unit.
8. (Currently Amended) The quantizer as claimed in ~~one of the preceding claims~~ claim 1, wherein a latch is provided as comparison unit (~~47~~).
9. (Currently Amended) The quantizer as claimed in ~~one of the preceding claims~~ claim 1, wherein the latch exhibits a comparator and a sample-and-hold device.
10. (Currently Amended) The quantizer as claimed in ~~one of the preceding claims~~ claim 1, wherein the quantizer (2) is constructed symmetrically with a positive and a negative signal path and correspondingly with a positive signal input (21a) for a positive input signal (INP) and with a negative signal input (21b) for a negative input signal (INN).
11. (Currently Amended) The quantizer as claimed in claim 8, wherein a degeneration resistor (~~5~~) is provided between a positive and a negative signal path.
12. (Currently Amended) The quantizer as claimed in ~~one of the preceding claims~~ claim 1, wherein a separate static threshold current source (~~49; 49a and 49b~~) is allocated to each quantizing cell.
13. (Currently Amended) A quantizer (1) for a sigma delta modulator (10) with at least one input stage (2), the quantizer (1) quantizing an input signal (21), which is present at its input stage, in accordance with at least one threshold signal (25) and outputting it as result value (22) at a digital result output (23), wherein the quantizer (1) contains at least one quantizing cell (40) corresponding to the number of its resolution levels, each quantizing cell (40) exhibiting a voltage comparator (61) which compares the input signal (21), present as input signal voltage (62), with an associated threshold signal

voltage $\{63_i\}$ and, if the input signal voltage exceeds or drops below the threshold signal voltage, outputs a corresponding digital result bit $\{0/1\}$ (Q_i), a digital adder $\{66\}$ being provided which adds the digital result value $\{22\}$ of the last weighting of the comparators of the quantizer $\{4\}$ to the individual threshold signal voltages of the comparators by incrementing or decrementing the threshold signal voltages by part voltages $\{25\}$ corresponding to the digital result value.

14. (Currently Amended) The quantizer as claimed in claim 13, wherein to each quantizing cell $\{40\}$, a threshold signal is allocated which differs from the threshold signals of other quantizing cells.
15. (Currently Amended) The quantizer as claimed in ~~one of claims 13 to 14~~ claim 13, wherein a reference voltage generator $\{65\}$ is provided which generates the threshold signal voltages $\{63_i\}$, which are different for each voltage comparator $\{64\}$, the threshold signal voltages being selectable in part voltages $\{25\}$.
16. (Currently Amended) The quantizer as claimed in ~~one of claims 13 to 15~~ claim 13, wherein the reference voltage generator $\{65\}$ is constructed by a chain of resistors $\{68\}$, the part voltages $\{25\}$ of which are assembled to form the threshold voltages $\{63_i\}$.
17. (Currently Amended) The quantizer as claimed in ~~one of claims 13 to 16~~ claim 13, wherein a switching mechanism is allocated to the adder $\{66\}$, which switching mechanism exhibits switches $\{67\}$, at the inputs of which the part voltages $\{25\}$ of the reference voltage generator $\{65\}$ are present and the outputs of which are connected to the inputs $\{V_{th_i}\}$ for the threshold signal voltages $\{63_i\}$ of the comparators $\{64\}$, the switches being controlled by the output signal $\{Add<0:6>\}$ of the adder.
18. (Currently Amended) The quantizer as claimed in ~~one of claims 13 to 17~~ claim 13, wherein the reference voltage generator $\{65\}$ generates the part voltages $\{25\}$ which can be applied to the respective comparator for weighting the input signal in accordance with the digital result value and/or the desired threshold signal voltage by means of switches $\{67\}$.
19. (Currently Amended) The quantizer as claimed in ~~one of claims 13 to 18~~ claim 13, wherein the result bits $\{Q_i\}$ together form the result value $\{22\}$.

20. (Currently Amended) The quantizer as claimed in ~~one of claims 13 to 19~~ claim 13, wherein the threshold signals exhibit fixed differences with respect to one another.
21. (Currently Amended) The quantizer as claimed in ~~one of claims 13 to 20~~ claim 13, wherein the quantizer (2) is constructed symmetrically with a positive and a negative signal path and correspondingly with a positive signal input (21a) for a positive input signal and with a negative signal input (21b) for a negative input signal.
22. (Currently Amended) The quantizer as claimed in ~~one of claims 13 to 24~~ claim 13, wherein the comparators (61) are formed by continuous-time voltage comparators.
23. (Currently Amended) The quantizer as claimed in ~~one of the preceding claims~~ claim 13, wherein a latch is provided which stores the result supplied by the comparators.
24. (Currently Amended) A sigma delta modulator (10) having at least one input stage (2) and with a quantizer (1) as claimed in ~~one of the preceding claims~~ claim 13.